

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	interrupt\$2 near4 (co?process\$3) near4 (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/04 15:45
S2	1	(interrupt\$2 near4 (co?process\$3)) with (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/04 15:44
S3	1	(interrupt\$2 near4 (co?process\$3)) same (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/04 15:44
S4	1	(interrupt\$2 near4 (co?process\$3)) and (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/04 15:44
S5	5	interrupt\$2 near4 (co?process\$3) near4 register\$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/04 16:48
S6	4876	(interrupt\$1 near4 (control\$4 or arbit\$3 or rout\$3 or APIC)) same (interrupt\$1 near4 register\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/04 16:50
S7	606	(interrupt\$1 near4 (control\$4 or arbit\$3 or rout\$3 or APIC)) same (interrupt\$1 adj1 register\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/04 16:50
S8	297	(712/214).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:45
S9	487	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:45
S10	56	((speculat\$5 or predict\$5) near4 issu\$3) with (pipelin\$3 near4 stag\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:55
S11	2	((speculat\$5 or predict\$5) near4 result\$1) with (pipelin\$3 near4 stag\$3) with (availab\$5 or ready or finish\$3 or complet\$3 or done)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:57

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S12	512	(712/218).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:57
S13	5	((speculat\$5 or predict\$5) near4 result\$1) with (forward\$3 or bypass\$3) with (pipelin\$3 near4 stag\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:59
S14	29453	((speculat\$5 or predict\$5) near4 result\$1) sane ((forward\$3 or bypass\$3) with (pipelin\$3 near4 stag\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:59
S15	17	((speculat\$5 or predict\$5) near4 result\$1) same ((forward\$3 or bypass\$3) with (pipelin\$3 near4 stag\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/28 11:59
S16	528	(712/218).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:46
S17	300	(712/214).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:47
S18	494	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:47
S19	15	confidence near4 valu\$2 near4 issu\$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:48
S20	1	interrupt\$2 near4 (co?process\$3) near4 (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:49
S21	1	(interrupt\$2 near4 (co?process\$3)) with (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:49
S22	1	(interrupt\$2 near4 (co?process\$3)) same (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:49
S23	1	(interrupt\$2 near4 (co?process\$3)) and (pseudo?instruction\$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:49

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S24	5	interrupt\$2 near4 (co?process\$3) near4 register\$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:49
S25	2	((speculat\$5 or predict\$5) near4 result\$1) with (pipelin\$3 near4 stag\$3) with (availab\$5 or ready or finish\$3 or complet\$3 or done)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:49
S26	5	((speculat\$5 or predict\$5) near4 result\$1) with (forward\$3 or bypass\$3) with (pipelin\$3 near4 stag\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:50
S27	17	((speculat\$5 or predict\$5) near4 result\$1) same ((forward\$3 or bypass\$3) with (pipelin\$3 near4 stag\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:50
S28	7	((("5872947") or ("5964867") or ("5923862") or ("6360315") or ("6144982") or ("6393550") or ("5958041"))).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/06/23 14:54



"Confidence value" + prediction + "pipeline stage"



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[PS] Selective dual path execution

TH Heil, JE Smith - Unpublished, University of Wisconsin-Madison, November, 1996 - ece.wisc.edu

... SDPE restricts the number of simultaneously executed paths to two, and uses a branch

**prediction** confidence mechanism to fork selectively only for branches that ...

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An Evaluation of Speculative Instruction Execution on Simultaneous Multithreaded Processors

- [group of 7](#) »

SJ EGGERS, HM LEVY - ACM Transactions on Computer Systems, 2003 - portal.acm.org

... 4. Per-pipeline-stage IPC for INT+FP, divided between correct-path-, wrong-path ... If

the **confidence value** is above the threshold, the **prediction** is followed ...

[Cited by 5](#) - [Web Search](#) - [BL Direct](#)

VALUE PREDICTION: Improving Instruction Level Parallelism

E Rotenberg, RT Miller, D Patel - tinker.ncsu.edu

... for the stride predictor method) entry, **confidence value**, and the ... case by doing Oracle

Store **Prediction** using the ... value is computed in the MEM1 **pipeline stage**. ...

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Characterizing the Performance of Value Prediction using Statistical Simulations

P Giese - webspace.ulbsibiu.ro

... Predicted Value **Confidence Value** & History File Correct Value Predicted Value First

Level Index Value History File Value **Prediction** File Update Queue ...

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[PS] Selective Dual Path Execution

THHJE Smith - ece.wisc.edu

... SDPE restricts the number of simultaneously executed paths to two, and uses a branch

**prediction** confidence mechanism to fork selectively only for branches that ...

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Using Statistical and Symbolic Simulation for Microprocessor Performance Evaluation

M Oskin, FT Chong, M Farrens - jilp.org

... instruction fetch mechanisms, branch **prediction**, code generation, and value **prediction**. ...

in terms of queue sizes and inter-pipeline stage bandwidth; however ...

[View as HTML](#) - [Web Search](#)

Exploiting Prediction to Reduce Power on Buses - [group of 10](#) »

V Wen, M Whitney, Y Patel, JD Kubiawicz - Proceedings of the 10th International Symposium on High ..., 2004 - doi.ieeecomputersociety.org

... The highest **confidence value** will be matched with a ... we subject it to different

**prediction** schemes to ... goes through an explicit **pipeline stage** in SimpleScalar. ...

[Cited by 3](#) - [Web Search](#)

Optimizing Inter-Instruction Value Communication through Degree of Use Prediction

JA Butts - 2004 - cs.wisc.edu

Page 1. Optimizing Inter-Instruction Value Communication through Degree of Use



"Confidence value" + prediction + issue

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Selective value **prediction** - group of 13 »

B Calder, G Reinman, DM Tullsen - ACM SIGARCH Computer Architecture News, 1999 - portal.acm.org  
... out-of-order processor can **issue** 16 operations ... instructions can now start providing **predictions**, and the ... the value table its **confidence value** is initialized to ...  
[Cited by 143](#) - [Web Search](#) - [BL Direct](#)

Molecular classification of multiple tumor types - group of 20 »

CH Yeang, S Ramaswamy, P Tamayo, S Mukherjee, RM ... - Bioinformatics, 2001 - bioinformatics.oupjournals.org  
... posed as a multi- class **prediction** problem in machine ... absolute value denotes the confidence of **prediction**. ... weighted voting algorithm the **confidence value** is c ...  
[Cited by 118](#) - [Web Search](#) - [BL Direct](#)

[PS] Selective dual path execution

TH Heil, JE Smith - Unpublished, University of Wisconsin-Madison, November, 1996 - ece.wisc.edu  
... 2 m -1 Page 5. Selective Dual Path Execution November 19, 1996 5 branch **prediction** problem completely by reversing all **predictions** in the low confidence set!). ...  
[Cited by 46](#) - [View as HTML](#) - [Web Search](#)

Effective **Prediction** of Web-user Accesses: A Data Mining Approach - group of 9 »

A Nanopoulos, D Katsaros, Y Manolopoulos - Proceeding of the Workshop WEBKDD 2001: Mining Log Data ... - dbserver.csie.ncku.edu.tw  
... 34]. The core **issue** in **prediction** is the development of an effective algorithm that deduces the future user \* Contact author. ...  
[Cited by 52](#) - [View as HTML](#) - [Web Search](#)

Transduction with Confidence and Credibility - group of 5 »

C Saunders, A Gammerman, V Vovk - 1999 - eprints.ecs.soton.ac.uk  
... The confidence in **prediction** can then be defined as ... eg  $k \geq 7$ ) Each solution of this problem yields Lagrange ... Not only do we obtain a **confidence value** for our ...  
[Cited by 35](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

... exploration of region-level value locality with integrated computation reuse and value **prediction** - group of 8 »

Y Wu, DY Chen, J Fang - ACM SIGARCH Computer Architecture News, 2001 - doi.ieeecomputersociety.org  
... conservatively as alias analysis is a known hard problem. ... based predictor has the highest **confidence value**, we hash ... an index to a value **prediction** table (VPT ...  
[Cited by 14](#) - [Web Search](#) - [BL Direct](#)

Large-scale **prediction** of Saccharomyces cerevisiae gene function using overlapping transcriptional ... - group of 11 »

LF Wu, TR Hughes, AP Davierwala, MD Robinson, R ... - Nature Genetics, 2002 - csb.yale.edu  
... approaches to functional **prediction** have several complicating **issues**. ... a functional label and a **confidence value**. A **prediction** algorithm then uses a collec ...  
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"Confidence value" + prediction + multithreaded



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[... exploration of region-level value locality with integrated computation](#)

[reuse and value \*\*prediction\*\* - group of 8 »](#)

Y Wu, DY Chen, J Fang - ACM SIGARCH Computer Architecture News, 2001 - doi.ieeecomputersociety.org

... the context-based predictor has the highest **confidence value**, we hash ... obtain an index

to a value **prediction** table (VPT ... Figure 4. **Multithreaded** microarchitecture ...

Cited by 14 - [Web Search](#) - [BL Direct](#)

[Boosting SMT performance by speculation control - group of 5 »](#)

K Luo, M Franklin, SS Mukherjee, A Sezne - Parallel and Distributed Processing Symposium., Proceedings ..., 2001 - ieeexplore.ieee.org

... Simultaneous **multithreading** (SMT) is a recently pro- posed **multithreaded** processor

design ... A low **confidence value** indicates that the **prediction** is likely ...

Cited by 14 - [Web Search](#) - [Library Search](#)

[An Evaluation of Speculative Instruction Execution on Simultaneous \*\*Multithreaded\*\* Processors - group of 7 »](#)

SJ EGGERS, HM LEVY - ACM Transactions on Computer Systems, 2003 - portal.acm.org

... The **confidence value** for a branch is the ... Speculative Instruction Execution on

Simultaneous **Multithreaded** Processors ... Branch **Prediction** Accuracy was 88% Wrong ...

Cited by 5 - [Web Search](#) - [BL Direct](#)

[Modeling value speculation - group of 7 »](#)

Y Sazeides - High-Performance Computer Architecture, 2002. Proceedings. ..., 2002 - ieeexplore.ieee.org

... **Prediction** and speculation [4, 10, 36] have been proposed as a means for alleviating

the impediments of control dependences by predicting the next PC of ...

Cited by 3 - [Web Search](#)

[An open software architecture for virtual reality interaction - group of 6 »](#)

G Reitmayr, D Schmalstieg - Proceedings of the ACM symposium on Virtual reality software ..., 2001 - portal.acm.org

... as a **prediction** for a changing **prediction** interval is ... Modules may be implemented

**multi-threaded** to avoid stal ... a time stamp and a **confidence value** to describe ...

Cited by 39 - [Web Search](#)

[Characterizing the Performance of Value \*\*Prediction\*\* using Statistical Simulations](#)

P Giese - webspace.ulbsibiu.ro

... **Value & History File** ... play a significant role in LOAD only **predictions** the upper ... While

the **multithreaded** experiments involved larger memory latencies of 1000 ...

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[Criticality Driven Energy Aware Speculation for Speculative \*\*Multithreaded\*\* Processors - group of 2 »](#)

R NAGPAL, A BHOWMIK - Lecture notes in computer science - cs.iitm.ernet.in

... Keywords: Speculative **multithreading**, instruction criticality ... execution modeling,

**prediction**, speculation control ... ulative **multithreaded** (SpMT) processors [5], [6 ...

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[Speculative \*\*Multithreaded\*\* Architectures](#)

N Chong - doc.ic.ac.uk



simultaneous multithreaded

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JL Lo, LA Barroso, SJ Eggers, K Gharachorloo, HM ... - ACM SIGARCH Computer Architecture News, 1998 - doi.ieeecomputersociety.org

... This paper examines the memory system behavior of database management systems on **simultaneous multi- threaded** processors. **Simultaneous multithreading** (SMT) [4 ...Cited by 122 - [Web Search](#) - [BL Direct](#)An analysis of operating system behavior on a **simultaneous multithreaded** architecture - group of 13 »

JA Redstone, SJ Eggers, HM Levy - ACM SIGPLAN Notices, 2000 - portal.acm.org

An Analysis of Operating System Behavior on a **Simultaneous Multithreaded** Architecture ... methodological strategy in the context of **simultaneous multithreading**. ...Cited by 39 - [Web Search](#) - [BL Direct](#)**Simultaneous** multithreading: maximizing on-chip parallelism - group of 58 »

DM Tullsen, SJ Eggers, HM Levy - International Conference on Computer Architecture, 1998 - portal.acm.org

... section presents performance results for **simultaneous multi- threaded** processors.We begin by defining several machine models for **simultaneous multithreading**. ...Cited by 721 - [Web Search](#) - [BL Direct](#)Software-directed register deallocation for **simultaneous multithreaded** processors - group of 18 »

JL Lo, SS Parekh, SJ Eggers, HM Levy, DM Tullsen - IEEE Transactions on Parallel and Distributed Systems, 1999 - doi.ieeecomputersociety.org

... 10, No. 9; SEPTEMBER 1999, pp. 922-933. Software-Directed Register Deallocation for **Simultaneous Multithreaded** Processors \* ... 2. **SIMULTANEOUS MULTITHREADING**. ...Cited by 36 - [Web Search](#) - [BL Direct](#)Symbiotic jobscheduling for a **simultaneous multithreaded** processor

A Snively, DM Tullsen - ACM SIGOPS Operating Systems Review, 2000 - portal.acm.org

... there is hardware support for **simultaneous** execution that ... also apply to other **multi-threaded** architectures 3 ... which features ne-grain **multithreading**, has fewer ...Cited by 30 - [Web Search](#)Soft real-time scheduling on **simultaneous multithreaded** processors - group of 7 »

R Jain, CJ Hughes, SV Adve - Real-Time Systems Symposium, 2002. RTSS 2002. 23rd IEEE, 2002 - ieeexplore.ieee.org

... Abstract **Simultaneous multithreading** (SMT) improves processor throughput by processing instructions from multiple threads each cycle. ...Cited by 32 - [Web Search](#)Exploiting Choice: Instruction Fetch and Issue on an Implementable **Simultaneous** Multithreading ... - group of 45 »